Terms used **I/O** and **placement** and **power** Found **16,045** of **131,734**

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1 The "PI" (placement and interconnect) system

Ronald L. Rivest

January 1982 **Proceedings of the nineteenth design automation conference**

Full text available: pdf(771.18 KB) Additional Information: full citation, abstract, references, citings, index terms

"PI" is an advanced LISP-based placement and interconnect system for custom NMOS or CMOS (single-layer metal) designs. When fully implemented, PI will handle placement of arbitrarily-sized rectangular modules, routing of power and ground, signal routing, and compaction. In this paper we briefly review the structure of PI, and present details on the signal-routing heuristics, focusing on the definition of "channels", the global router, the "crossing placer" ...

2 ASIC design in nanometer era - dead or alive?: Designing mega-ASICs in nanogate technologies

David E. Lackey, Paul S. Zuchowski, Juergen Koehl

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(264.47 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses challenges the designer faces in integrating entire system product designs, containing tens or even hundreds of millions of logic gates, into single chip solutions now within reach using circuit densities possible in the latest silicon technologies. Managing designs of this size presents a new dimension of issues, and managing the physical and electrical effects of these high density device geometries presents another; solutions in both these areas are presented. Lastly, thi ...

Keywords: design productivity, methodology, power management, signal integrity, system-on-chip, time to market

3 Parallel I/O for scientific applications on heterogeneous clusters: a resource-utilization approach

Yong E. Cho, Marianne Winslett, Szu-wen Kuo, Jonghyun Lee, Ying Chen

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.30 MB) Additional Information: full citation, references, index terms

4 Power distribution issues: Macro-modeling concepts for the chip electrical interface

Brian W. Amick, Claude R. Gauthier, Dean Liu

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(515.95 KB) Additional Information: full citation, abstract, references, index terms

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

5 APSS: An automatic PLA synthesis system

M. W. Stebnisky, M. J. McGinnis, J. C. Werbickas, R. N. Putatunda, A. Feller

June 1983 **Proceedings of the twentieth design automation conference on Design automation**

Full text available: pdf(611.47 KB) Additional Information: full citation, abstract, references, citings, index terms

An integrated, fully automatic software capability that combines Boolean logic translation, Boolean minimization, PLA folding, PLA topology generation, and automatic PLA subchip interfacing to the MP2D standard cell automatic placement and routing program in a single, modular software package is described. Written in ANSI standard FORTRAN, APSS permits the designer to input either arbitrarily formed Boolean equations or a truth table, and to receive a complete MP2D-compatible PLA subchip la ...

6 Proud: a fast sea-of-gates placement algorithm

Ren-Song Tsay, Ernest S. Kuh, Chi-Ping Hsu

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(665.37 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a fast and effective placement algorithm which takes advantage of inherent scarcity in the connectivity specification. It solves repeatedly sparse linear equations by the SOR (Successive Over-Relaxation) method in a top-down hierarchy. The algorithm has been implemented; for a triple-metal-layer 100K sea-of-gates design with 26,000 instances, it takes 50 minutes on a VAX 8650 and yields excellent results.

7 An experimental system for power/timing optimization of LSI chips

B. J. Agule, J. D. Lesser, A. E. Ruehli, P. K. Wolff

January 1977 **Proceedings of the 14th design automation conference**

Full text available: pdf(423.02 KB) Additional Information: full citation, abstract, references, citings, index terms

An experimental system of programs is described which places logic gates on a chip, globally wires the gates and then optimizes the power required to drive them. Further power reductions are realized by using power-oriented placement improvement techniques. A companion paper describes how the optimization is accomplished by using the timing requirements of the chip as constraints and assigning delays to the logic gates so that these constraints are met and the power is minimized.

8 Power supply noise analysis methodology for deep-submicron VLSI chip design

Howard H. Chen, David D. Ling

June 1997 **Proceedings of the 34th annual conference on Design automation conference**

Full text available: pdf(237.07 KB) Additional Information: full citation, references, citings, index terms

9 Development of ASIC Chip-Set for High-End Network Processing Application-A Case Study

Sanjeev Patel

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(169.08 KB) Publisher Site Additional Information: full citation, abstract

Choosing the right methodology is a significant step towards successful VLSI designs. Traditional methodologies and tools are no longer adequate to handle large and complex designs. This paper presents a novel design methodology for complex deep-submicron designs, using a case study of the development of a high-end network processing ASIC chip-set. The paper focuses on the synergetic use of the "dual design verification approach", along with static verification methods in achieving defect free s ...

10 A flat, timing-driven design system for a high-performance CMOS processor chipset

J. Koehl, U. Baur, T. Ludwig, B. Kick, T. Pflueger

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(155.54 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe the methodology used for the design of the CMOS processor chipset used in the IBM S/390 Parallel Enterprise Server - Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm2 is comparable to the most advanced custom designs and that the impact of interconnect d ...

11 Placement: I/O placement for FPGAs with multiple I/O standards

Wai-Kei Mak

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(90.42 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present the first exact algorithm to solve the constrained I/O placement problem for FPGAs that support multiple I/O standards. We derive a compact integer linear programming formulation for the constrained I/O placement problem. The size of the integer linear program derived is independent of the number of I/O objects to be placed and hence is scalable to very large design instances. For example, for a Xilinx Virtex-E FPGA, the number of integer variables required is never mor ...

Keywords: I/O placement, I/O standards, field-programmable gate array, placement

12 Hierarchical physical design methodology for multi-million gate chips

Wei-Jin Dai

April 2001 **Proceedings of the 2001 international symposium on Physical design**

Full text available: pdf(136.52 KB) Additional Information: full citation, abstract, citings, index terms

In this paper, a design methodology for the implementation of multi-million gate system-on-chip designs is described.

Keywords: deep sub-micron, floorplanning, hierarchical design, partitioning, physical prototype, placement

13 EMI-noise analysis under ASIC design environment

Sachio Hayashi, Masaaki Yamada

April 1999 **Proceedings of the 1999 international symposium on Physical design**

Full text available: pdf(912.47 KB) Additional Information: full citation, references, index terms

14 Challenges in the Design of a Scalable Data-Acquisition and Processing System-on-Silicon

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(155.29 KB) Publisher Site Additional Information: full citation, abstract

Increasing complexity of the functionalities and the resultant growth in number of gates integrated in a chip coupled with shrinking geometries and short cycle time requirements bring in several challenges into the design of present day VLSI chips. In this paper we present the challenges faced and the approaches successfully adopted in the design of a complex 2.5 million gate high bandwidth data acquisition and processing VLSI chip (a trace-receiver chip, code-named Drishti) in a deep sub-micron ...

15 An efficient layout style for 2-metal CMOS leaf cells and their automatic generation

Chi-Yi Hwang, Yung-Ching Hsieh, Youn-Long Lin, Yu-Chin Hsu

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation conference**

Full text available: pdf(750.81 KB) Additional Information: full citation, references, citings, index terms

16 Robust IP watermarking methodologies for physical design

Andrew B. Kahng, Stefanus Mantik, Igor L. Markov, Miodrag Potkonjak, Paul Tucker, Huijuan Wang, Gregory Wolfe

May 1998 **Proceedings of the 35th annual conference on Design automation conference**

Full text available: pdf(425.94 KB) Additional Information: full citation, abstract, references, citings, index terms

Increasingly popular reuse-based design paradigms create a pressing need for authorship enforcement techniques that protect the intellectual property rights of designers. We develop the first intellectual property protection protocols for embedding design watermarks at the physical design level. We demonstrate that these protocols are tarnsparent with respect to existing industrial tools and design flows, and that they can embed watermarks into real-world industrial designs ...

17 Papers: On the origin of power laws in Internet topologies

Alberto Medina, Ibrahim Matta, John Byers

April 2000 **ACM SIGCOMM Computer Communication Review**, Volume 30 Issue 2

Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings

Recent empirical studies [6] have shown that Internet topologies exhibit power laws of the form $y = x^{a}$ for the following relationships: (P1) outdegree of node (domain or router) versus rank; (P2) number of nodes versus outdegree; (P3) number of node pairs within a neighborhood versus neighborhood size (in hops); and (P4) eigenvalues of the adjacency matrix versus rank. However, causes for the appearance of such power laws have not been convincingly given. In this ...

18 PLAY: pattern-based symbolic cell layout: Part I: transistor placement

W.-J. Lue, L. P. McNamee

October 1987 **24th ACM/IEEE conference proceedings on Design automation conference**

Full text available: pdf(857.09 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes an approach to symbolic transistor placement from a CMOS circuit net-list as part of an automatic custom cell layout system, PLAY. It consists of two parts, extraction and refinement. The extraction process defines a set of patterns using local connection relationships. Refinement procedures assign topological attributes to each transistor through these patterns and relationships along with other heuristic knowledge. This paradigm provi ...

19 Probing the black box: Transforming policies into mechanisms with infokernel

Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau, Nathan C. Burnett, Timothy E. Denehy, Thomas J. Engle, Haryadi S. Gunawi, James A. Nugent, Florentina I. Popovici

October 2003 **Proceedings of the nineteenth ACM symposium on Operating systems principles**

Full text available: pdf(365.12 KB) Additional Information: full citation, abstract, references, index terms

We describe an evolutionary path that allows operating systems to be used in a more flexible and appropriate manner by higher-level services. An infokernel exposes key pieces of information about its algorithms and internal state; thus, its default policies become mechanisms, which can be controlled from user-level. We have implemented two prototype infokernels based on the linuxtwofour and netbsdver kernels, called infolinux and infobsd, respectively. The infokernels export key abstractions as ...

Keywords: information, mechanism, policy

20 Standard cell placement for even on-chip thermal distribution

Ching-Han Tsai, Sung-Mo (Steve) Kang

April 1999 **Proceedings of the 1999 international symposium on Physical design**

Full text available: pdf(723.75 KB) Additional Information: full citation, references, index terms

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